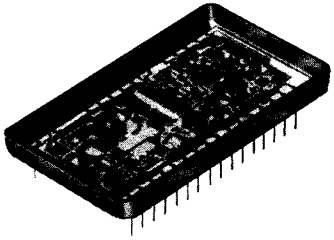
12 BIT 2μSEC HYBRID A/D CONVERTERS
Low cost, military, standard pin out

A



FEATURES

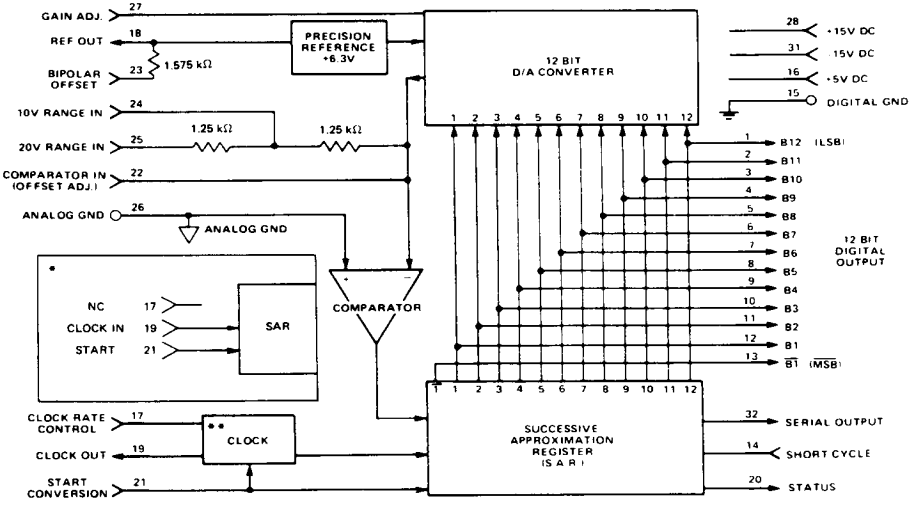
- *2 μSEC CONVERSION TIME*
- *12 BIT RESOLUTION AND LINEARITY*
- *LOW COST*
- *HIGHER SPEED PIN FOR PIN REPLACEMENT FOR ADC87 TYPES (NO BUFFER)*
- *32 PIN TDIP HERMETIC HYBRID*

DESCRIPTION

The ADC-00403 is a 12 bit 2 microsecond hybrid A/D converter packaged in a hermetic 32 pin TDIP. It offers a low cost higher speed pin for pin replacement for ADC87 and ADC85 types. Offered in models with internal (ADC-00404) or external (ADC-00403) clock, it also features precision internal reference, 6 pin programmable input voltage ranges, and both serial and parallel data output.

APPLICATIONS

With its low cost, high speed and small hermetic package, the ADC-00403 is ideal for most military and industrial data conversion applications. Typical of these applications are vibration and FFT analysis, sonar and radar digitizing, medical and nuclear instrumentation, and multiplexed data acquisition systems.



*Function for ADC-00403 model only.
**Function for ADC-00404 model only.

FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS

Typical values at + 25°C case temperature and nominal power supply voltages

PARAMETER	UNITS	VALUES 10 BIT LIN	VALUES 12 BIT LIN
RESOLUTION	Bits	12	12
ACCURACY AND DYNAMICS			
Linearity Error	% of F.S.R.	±0.048 max	±0.012 max
Linearity Error Tempco	ppm/°C	±5 max	±2 max
Gain Error (Trimmable to zero)	% of F.S.R.	±0.1	±0.1
Gain Error Tempco	ppm/°C	±25	±15
Offset (Trimmable to zero)			
Unipolar	% of F.S.R.	±0.05 typ	±0.05 typ
Bipolar	% of F.S.R.	±0.1 typ	±0.1 typ
Offset Tempco			
Unipolar	ppm/°C	±3 max	±3 max
Bipolar	ppm/°C	±10 max	±7 max
Diff. Linearity Error	LSB	±1	±1
Conversion Time*	µs	1.5 max	2.0 max
Cycle Time*	µs	1.7 max	2.2 max
* The internal clock frequency is controlled by the applied Clock Rate Control voltage. See figure 4.			
ANALOG INPUTS			
Input Ranges			
Unipolar	V	0 to +5; 0 to +10; 0 to +20	
Bipolar	V	±2.5; ±5; ±10	
Max Voltage Without Damage		See figure 6.	
Impedance			
0 to +5V and ±2.5V	KΩ	0.625	
0 to 10V and ±5V	KΩ	1.25	
±10V	KΩ	2.50	
DIGITAL INPUTS			
Start Convert	nsec	50 min positive pulse. Trailing edge initiates conversion	
Loading	TTL loads	1	
DIGITAL OUTPUTS			
Parallel Data		Bit 1 through Bit 12 plus $\overline{MSB}$	
Drive	TTL loads	5	
Unipolar Coding		Complementary binary	
Bipolar Coding		Complementary offset binary or Complementary two's complement	
Serial Data		Non return to zero (NRZ)	
Drive	TTL loads	5	
Coding		Same as parallel data	
Status		Logic "1" during conversion. Logic "0" indicates valid parallel data.	
Drive	TTL loads	2	
Clock		13 positive pulses	
Period*	nsec	166 min	
Drive	TTL loads	2	
INTERNAL REFERENCE			
Voltage Output	V	+6.2 ±5%	
Current Output	mA	5 max for no degradation of specifications	
Voltage Tempco	ppm/°C	±20 max	
POWER SUPPLIES			
Voltages	V	+15 ±5%	−15 ±5% / +5 ±5%
Max Voltage Without Damage	V	+18	−18 / +7
Current (Including Internal Clock)	mA	50 typ / 60 max	65 typ / 80 max / 165 typ / 220 max
Sensitivity	%FSR/%PS	±0.002	±0.002 / ±0.002
TEMPERATURE RANGE			
Operating (Case)			
-1 Option	°C	−55 to +125	
-2 Option	°C	−25 to +85	
Storage	°C	−65 to +135	
PACKAGE			
Type		32 pin TDIP	
Size	Inch (mm)	1.16 x 1.95 x 0.2 (29.34 x 49.4 x 5.0)	
Weight	Oz. (g)	0.67 (19)	

BLOCK DIAGRAM DESCRIPTION

Figure 1 is a block diagram of the ADC-00403. Since the ADC-00403 is a successive approximation A/D converter, its main elements are a D/A Converter, a Comparator and a Successive Approximation Register. An Internal Precision Reference and internal or external Clock, depending on model selected, complete the functional elements of the ADC-00403.

The successive approximation algorithm is initiated by a Start Conversion pulse input. This results in a change of the Status output signal, indicating that a conversion is in progress and output data is invalid. In a sequence starting with Bit 1, the D/A input is set to "1" and the comparator detects whether the resulting D/A output is larger or smaller than the analog input signal. If the D/A output is larger than the analog input signal, Bit 1 is reset to "0". If not, then Bit 1 remains a "1". In succession, Bit 2 through Bit 12 are individually tested by the comparator. After 12 trials, and 13 clock pulse edges have occurred, the Successive Approximation Register (SAR) output is a digital representation of the analog input. At this time, the Status output signal changes to indicate that conversion has been completed and output data is valid.

The ADC-00403 is available in both internal clock or external clock models. The internal clock model makes the clock signal available to the user on the Clock Output pin. In addition, the Clock Rate Control input pin may be used to make fine adjustments of the internal clock frequency. The ADC-00403 may be short cycled for less than 12 bit resolution with a resulting decrease in its conversion time.

Both parallel data and serial data are provided as digital outputs from the converter. For bipolar analog input signals the digital output data is coded in Complementary Two's Complement or Complementary Offset Binary. Both Bit 1 and Bit 1 complement ($\overline{B1}$) are provided as outputs, so either of these codes may be selected. For unipolar analog input signals, the digital output data is coded in Complementary Binary.

The ADC-00403 may be configured for any of six different input signal ranges by means of jumper wires between pins. Three bipolar and three unipolar ranges are implemented with combination of the two precision scaling resistors and the precision bipolar offset resistor. Inherent offset and gain errors of the A/D converter may be trimmed to zero with the addition of potentiometers.

The ADC-00403 contains an internal precision +6.2 volt reference. This reference voltage is provided for the user at an output pin. In order to avoid affecting converter performance, care must be taken not to load the reference beyond its output capability.

To achieve the optimum performance available from the ADC-00403, it is recommended that decoupling capacitors be used on the supply lines. In addition, high frequency layout considerations should be kept in mind when designing a printed circuit board to accomodate the A/D converter. This includes minimum conductor lengths on signals, and a low impedance ground plane where possible.

TIMING DIAGRAM

A diagram of typical A/D converter timing is shown in Figure 2. A conversion is initiated by the application of a positive (50 nsec min) pulse to the Start Convert pin. A delayed (25 nsec min) clock must be applied to the Clock In pin for model ADC-00403. For model ADC-00404 the Clock Output appears after the falling edge of the Start Convert pulse. The rising edge of the clock causes the status signal to change to a "1", indicating that a conversion is in progress and parallel output data is not valid. Also in response to the clock rising edge, the MSB of the Successive Approximation Register (SAR) is reset to "0" and all other bits are set to "1". During clock period 1, the MSB trial takes place, and the MSB bit weight is compared to the analog input. The rising edge of clock pulse 2 causes the decision of the MSB trial to be stored, and simultaneously initiates the Bit 2 trial. In a successive manner, the rising edge of clock pulses 3 through 13 cause the storage of decisions on Bit 2 through Bit 12. The rising edge of clock pulse 13 causes the status signal to change to a "0", since the SAR now contains the valid 12 bit representation of the analog input. Parallel output data is valid during the interval that status signal is "0".

Serial Data is available as an output in non return to zero (NRZ) format. Data for each bit becomes valid on the rising edge of the clock pulse one number higher than the bit number, and remains valid for one clock period. Typically, Serial Data is shifted into an external 12 bit shift register, using the falling edges of the clock signal. The falling edge of clock pulse 13 would therefore shift Bit 12 into the register.

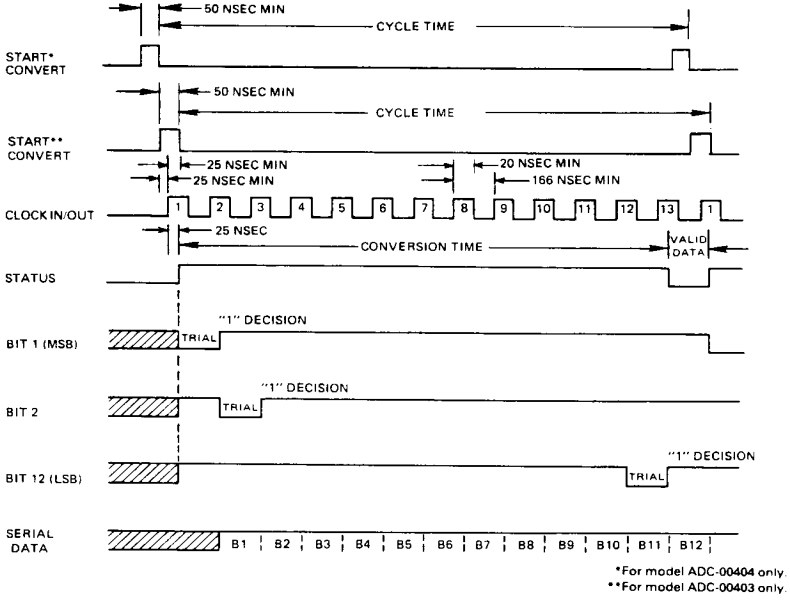
The minimum clock period allowed for rated performance of the ADC-00403 is 166 nanoseconds. This applies to both internal clock and external clock models. Conversion time is defined as the time during which the Status signal is a "1" and parallel output data is not valid. Cycle time, which is slightly longer than conversion time, is defined as the minimum time which must elapse between successive Start Convert pulses.

EXTERNAL CLOCK

The ADC-00403 is available in internal and external clock models. For external clock models the user must provide a clock signal to Clock Input (pin 19). Thirteen positive clock pulses are required to complete the conversion process. For rated A/D performance, the applied clock period must be 166 nanoseconds minimum. Figure 2 shows Clock In timing relationships. Best performance is achieved with a clock "high" duty cycle of between 12% and 33%. This sequence initiates conversions for both gated clock and continuous clock inputs. Care must be taken to comply with the minimum cycle time requirement between successive Start Convert pulses.

SHORT CYCLING AND CONTINUOUS CONVERSION

The ADC-00403 may be short cycled to fewer than 12 bits resolution, with a resulting decrease in conversion time. Figure 3 shows the required jumper connections and the resulting conversion times, with a 6 MHz clock, for 8 bit through 12 bit resolutions. For resolutions of less than 12 bits, it is possible to increase the clock frequency somewhat, since internal settling times are shorter. This may be accomplished by adjusting the Clock Rate Control voltage.



*For model ADC-00404 only.
**For model ADC-00403 only.

FIGURE 2. TIMING DIAGRAM

The ADC-00403 can be simply configured for continuous conversion operation when it is required. The falling edge of the Status (pin 20) signal is used to trigger a one shot. The one shot output, a 50 nsec minimum positive pulse, is connected to the Start Convert (pin 21) input to yield continuous conversion operation.

CLOCK RATE CONTROL

The Clock Rate Control line is made available in the internal clock model of the ADC-00404 to make small adjustments of the internal clock frequency. Figure 4 shows a typical circuit using a potentiometer to generate the Clock Rate Control voltage, and the resulting clock frequencies. For 12 bit operation, care must be taken to comply with the 166 nanosecond minimum clock period requirement. For short cycled operation, the Clock Rate Control voltage may be set greater than 5 volts, resulting in a clock frequency greater than 8 MHz.

PARALLEL DATA

Bit 1 through Bit 12 plus $\overline{\text{MSB}}$ are the parallel output data lines provided by the ADC-00403. Each signal can drive a minimum of 5 standard TTL loads. Parallel output data is valid during the time that the Status signal is a "0". If a strobe signal is required to read the parallel data into a register a "one-shot" can be triggered by the falling edge of the Status signal, or the falling edge of clock pulse 13 can be isolated by gating the Clock and Status signals together.

SERIAL DATA

Serial Data is provided by the ADC-00403 in non return to zero (NRZ) format with the MSB first. The Serial Data output line can drive a minimum of 2 standard TTL loads.

Each bit becomes valid on the rising edge of the clock pulse one number higher than the bit number, and remains valid for one clock period. Typically an external 12 bit shift register is used to store the serial data, after it has been shifted into the register using the falling edges of the clock signal. The LSB would be shifted into the register by the falling edge of clock pulse 13.

OUTPUT CODING

The ADC-00403 provides Complementary Binary coded output data for unipolar analog inputs, and either Complementary Offset Binary or Complementary Two's Complement coded output data for bipolar analog inputs. Figure 5 illustrates the output data for various analog inputs for each of the three code configurations. For bipolar analog inputs, the 2 choices of output code are available since both MSB and $\overline{\text{MSB}}$ signals are provided as outputs.

ANALOG INPUT RANGES

The ADC-00403 may be configured for any of six different input signal ranges by means of jumper wires between pins. Three bipolar and three unipolar ranges are possible. Figure 6 shows these six choices of analog input range, along with the jumper connections required to implement each range. The chart also shows, for each input range, which pin is to be used for the input signal, and what impedance will be presented at that pin. Absolute maximum input voltage is also shown for each configuration.

RESOLUTION	CONNECT PIN 14 TO	CONVERSION TIME
8 BIT	PIN 4	1.3 μsec
9 BIT	PIN 3	1.5 μsec
10 BIT	PIN 2	1.6 μsec
11 BIT	PIN 1	1.8 μsec
12 BIT	NC	2.0 μsec

FIGURE 3. SHORT CYCLE OPERATION

PIN 17 VOLTAGE	APPROXIMATE CLOCK RATE
+5V	8 MHz
0V	6 MHz

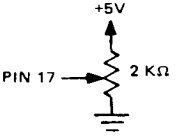


FIGURE 4. CLOCK RATE CONTROL

SCALE	BIPOLAR		UNIPOLAR
	COMPLEMENTARY OFFSET BINARY	COMPLEMENTARY TWO'S COMPLEMENT	COMPLEMENTARY BINARY
+FS-1 LSB	0000 0000 0000	1000 0000 0000	0000 0000 0000
+3/4 FS	0001 1111 1111	1001 1111 1111	0011 1111 1111
+1/2 FS	0011 1111 1111	1011 1111 1111	0111 1111 1111
+1 LSB	0111 1111 1110	1111 1111 1110	1111 1111 1110
0	0111 1111 1111	1111 1111 1111	1111 1111 1111
− 1 LSB	1000 0000 0000	0000 0000 0000	
−1/2 FS	1011 1111 1111	0011 1111 1111	
−3/4 FS	1101 1111 1111	0101 1111 1111	
−FS	1111 1111 1111	0111 1111 1111	

FIGURE 5. OUTPUT CODING

INPUT RANGE	ABSOLUTE MAX INPUT	INPUT IMPEDANCE (OHMS)	INPUT TERMINAL	JUMPER CONNECTION
±2.5V	±3.75V	0.625 K	PIN 24	PIN 23 TO PIN 22 PIN 25 TO PIN 22
0 to +5V	+7.5V	0.625 K	PIN 24	PIN 23 TO PIN 26 PIN 25 TO PIN 22
±5V	±7.5V	1.25K	PIN 24	PIN 23 TO PIN 22
0 to +10V	+15V	1.25 K	PIN 24	PIN 23 TO PIN 26
±10V	±15V	2.5K	PIN 25	PIN 23 TO PIN 22
0 to +20V	30V	2.5 K	PIN 25	PIN 23 TO PIN 26

FIGURE 6. ANALOG INPUT RANGE

OFFSET AND GAIN TRIMS

Gain and offset errors of the ADC-00403 are factory trimmed to be less than the values listed in the specification table. The converter is externally trimmable to zero gain and zero offset error, providing the user with flexibility for applications requiring maximum performance.

Figure 7 illustrates the external trim potentiometer circuit connections required to adjust the gain and offset errors of the ADC-00403 to zero. Multi-turn trimpots, with temperature coefficient of less than 100 ppm/°C, are recommended for best performance.

If gain adjust pot is not used, connect Gain Adjust pin 27 to Analog Gnd pin 26 to minimize noise.

INTERNAL REFERENCE

The ADC-00403 contains a +6.3 volt precision internal reference, which is made available for external use. A maximum output current of 5 mA will be provided by the internal reference, while maintaining rated performance. If this load is exceeded, gain and linearity error will increase. Damage will result from excessive loading.

LAYOUT PRECAUTIONS

To achieve the optimum performance of the ADC-00403, care must be taken in the printed circuit layout. Analog input lines and digital output lines should be separated from each other, and made as short as possible. To minimize ground noise, analog and digital grounds should be connected together in close proximity to the unit. A low impedance ground plane under the converter will yield the best results.

POWER SUPPLY DECOUPLING

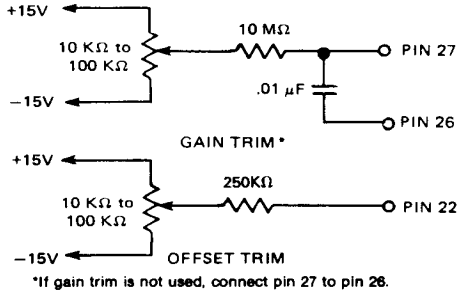
Capacitive decoupling of all power supplies is required to minimize noise. Figure 8 shows the recommended power supply decoupling configuration. Tantalum or electrolytic capacitors of 1 μF or greater are used for low frequency decoupling. Ceramic capacitors of 0.01 μF or greater are used for high frequency decoupling. For best results, all capacitors should be placed as close to the unit as possible.

ACCURACY TESTING

Testing of the accuracy of the ADC-00403 consists of measurement of its gain, offset and linearity errors. Figure 9 shows a simple test circuit for making these measurements. A precision DC voltage source is used to provide the analog input signal, and the digital outputs are monitored by a string of light emitting diodes (LED).

The offset error can be measured by adjusting the DC voltage source until the LEDs indicate the zero code transition. The difference between the voltage input and zero volts is the offset error. After the offset error has been measured, the circuit shown in Figure 7 should be used to trim the offset error to zero.

With the offset error trimmed to zero, the gain error can be measured by adjusting the DC voltage source until the LEDs indicate the full scale code transition. The difference between the input voltage and the theoretical full scale input is the gain error. After the gain error has been measured, the circuit shown in Figure 7 should be used to trim the gain error to zero.



*If gain trim is not used, connect pin 27 to pin 26.

FIGURE 7. OFFSET AND GAIN TRIM

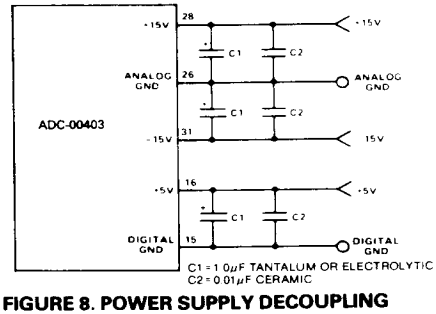


FIGURE 8. POWER SUPPLY DECOUPLING

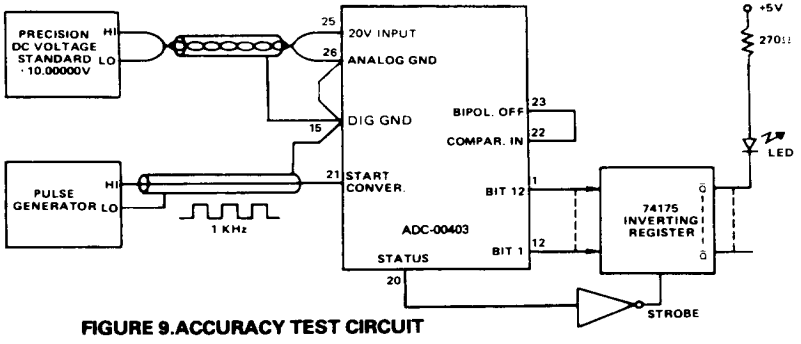


FIGURE 9.ACCURACY TEST CIRCUIT

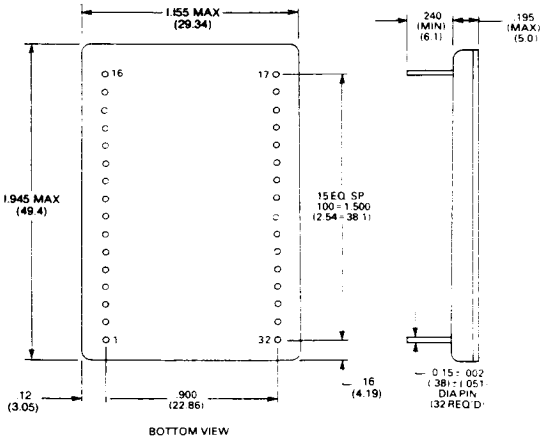
With the offset and gain errors trimmed to zero, any remaining error is a linearity error. Linearity error should be measured at the code transitions corresponding to each individual bit weight, and also at each of the major carry code transitions which occur at one count less than the individual bit weights.

PIN FUNCTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	Bit 12 (LSB)	17	NC*/Clk Rate Control**
2	Bit 11	18	Ref. Out (+6.2V)
3	Bit 10	19	Clock In*/Clock Out**
4	Bit 9	20	Status
5	Bit 8	21	Start Convert
6	Bit 7	22	Comparator In
7	Bit 6	23	Bipolar Offset
8	Bit 5	24	10V Range In
9	Bit 4	25	20V Range In
10	Bit 3	26	Analog Gnd
11	Bit 2	27	Gain Adjust
12	$\overline{\text{Bit 1 (MSB)}}$	28	+15V Supply
13	Bit 1 (MSB)	29	NC
14	Short Cycle	30	NC
15	Dig. Gnd	31	−15V Supply
16	+5 V Supply	32	Serial Out

*Function for ADC-00403 model only.
**Function for ADC-00404 model only.

MECHANICAL OUTLINE
32 PIN TRIPLE DIP



NOTES
1. Dimensions shown are in inches. (millimeters)
2. Lead identification numbers are for reference only
3. Lead spacing dimensions apply only at seating plane
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

ORDERING INFORMATION

ADC-00403-103

Linearity Grade:
3 = 12 bit (0.012% FSR)

Reliability Grade:
0 = Standard DDC procedures.
1 = 883B Processing.
2 = 883B Processing but without QCI testing.

Operating Temperature Range (Case)
1 = −55°C to +125°C
2 = −25°C to +85°C

Clock Option
3 = External Clock
4 = Internal Clock

H